REMARKS

The foregoing amendments and the following remarks are responsive to the August 19, 2004 Office Action. Claims 2, 4-7. 9-16, 18, and 19 remain as originally filed, Claim 3 is cancelled without prejudice, and Claims 1, 8, 17, and 20 are amended. Thus, Claims 1, 2, and 4-20 are presented for further consideration. Please enter the amendments and reconsider the claims in view of the following remarks.

Response to Rejection of Claims 3 and 20 Under 35 U.S.C. § 112, Second Paragraph

In the August 19, 2004 Office Action, the Examiner rejects Claims 3 and 20 as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. As described herein, Applicants have cancelled Claim 3 without prejudice. Applicants have also amended Claim 20 to depend from Claim 19. Applicants submit that amended Claim 20 has proper antecedent basis, and Applicants respectfully request the Examiner to withdraw the rejection of Claim 20 and to pass Claim 20 to allowance.

Response to Rejection of Claims 1, 2, 4-6, 8-12, and 17-19 Under 35 U.S.C. § 102(e)

In the August 19, 2004 Office Action, the Examiner rejects Claims 1, 2, 4-6, 8-12, and 17-19 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,594,167 issued to Yamasaki et al. ("Yamasaki").

Claim 1

As described herein, Applicants have amended Claim 1 to recite (emphasis added):

> 1. (Currently Amended) A memory module comprising:
>
> a printed circuit board having an edge, a first side, and a common signal trace connector area positioned along the edge, the printed circuit board having a plurality of interconnection levels;
>
> a first row of integrated circuits identical to one another, ...;
>
> a second row of integrated circuits identical to the integrated circuits of the first row, ...;
>
> a first plurality of data lines electrically connecting data pins of the first row of integrated circuits to the common signal trace connector area, each data line of the first plurality of data lines comprising trace portions on different interconnection levels of the printed circuit board, each trace portion having a trace portion length; and
>
> a second plurality of data lines electrically connecting data pins of the second row of integrated circuits to the common signal trace connector area, each data line of the second plurality of data lines comprising trace portions on different interconnection levels of the printed circuit board,

> each trace portion having a trace portion length, each data line having a length substantially equal to a sum of the trace portion lengths of the data line, whereby lengths of corresponding data lines of the first plurality of data lines and the second plurality of data lines are substantially the same.

FIGURES 4A-4C and paragraphs [0030]-[0032] of the present application illustrate certain embodiments of the invention recited by amended Claim 1 which have a primary signal layer 400, a MID1 signal layer 430, and a MID2 signal layer 460. Paragraph [0031] of the present application explains that (emphasis added):

> a signal trace 404 to one of the data pins of the U1 integrated circuit is designed to have substantially the same length from the data pin of the U1 integrated circuit to the primary memory module connector 420 as the length of a signal trace 414 from the corresponding data pin in the U11 integrated circuit to the primary memory module connector 420. The signal trace 404 from the U1 integrated circuit to the primary memory module connector 420 and the signal trace 414 from the U11 integrated circuit to the primary memory module connector 420 each include a respective portion of signal trace located on the MID2 layer 460 of the printed circuit board 104, as illustrated in FIGURE 4C.

As further described by the present application at paragraphs [0034]-[0035] (emphasis added):

> The overall lengths of the traces are configured to be substantially equal (to within 10% of the total trace length) by varying the lengths of the portions of the traces located on the MID1 layer 430 and the MID2 layer 460. In addition to the data signal trace lengths, the data mask trace lengths and the clock trace lengths advantageously are maintained to be substantially equal.
>
> Unlike known memory module circuit board designs, the substantial equality of trace lengths is achieved without requiring the addition of repetitious back-and-forth (i.e., serpentine) trace portions ... . Since printed circuit board 104 space is not consumed with serpentine signal traces, the signal traces are advantageously wider, and the spacing between signal traces is advantageously greater. The greater width and spacing of the signal traces advantageously results in decreased signal noise and interference. The absence of serpentine signal traces advantageously results in a memory module 100 that produces less radio frequency interference and is less susceptible to radio frequency interference.

In the cited paragraphs, the present application describes embodiments in which the corresponding data lines to an integrated circuit of the first row and to an integrated circuit of the second row have substantially equal lengths achieved by using trace portions on multiple interconnection levels of the printed circuit board. Such configurations provide benefits not found in the prior art configurations.

Applicants submit that Yamasaki does not disclose the recited structure of amended Claim 1. Yamasaki discloses (e.g., at column 7, lines 11-21) a memory module which has two

parallel rows of memory integrated circuits on opposite sides of a center line of the printed circuit board, with the memory chips angularly positioned such that data I/O pin groups DP are nearest to the center line. Yamasaki further discloses (e.g., at column 7, lines 28-33) that the distances from the data I/O pin groups DP to the module connector pins are substantially equal to one another. Yamasaki also discloses (e.g., at column 6, lines 59-64 and column 8, lines 16-45) that the data I/O pin groups DP are connected to the module connector pins via through-holes to an interconnection layer which is between the front and rear sides of the printed circuit board. Yamasaki does not disclose "each data line of the first plurality of data lines comprising trace portions on different interconnection levels of the printed circuit board, each trace portion having a trace portion length" and "each data line of the second plurality of data lines comprising trace portions on different interconnection levels of the printed circuit board, each trace portion having a trace portion length, each data line having a length substantially equal to a sum of the trace portion lengths of the data line, wherein lengths of corresponding data lines of the first plurality of data lines and the second plurality of data lines are substantially the same."

Yamasaki does not suggest the claimed invention of the present application because Yamasaki provides only limited capability to equate data line lengths of integrated circuits in the two rows of the memory module. Yamasaki is only able to substantially equate data line lengths for data pins which are close to the center line of the printed circuit board. For data pins farther from the center line, the configuration disclosed by Yamasaki is less and less successful in substantially equating the data line lengths. For example, Figures 5, 6, 11A, 11B, 13, 14, 17, and 19 of Yamasaki each show that only those data pins which are in proximity to the center line have data line lengths which are substantially equal.

The configurations disclosed by Yamasaki cannot reduce the difference between the data line lengths to be smaller than the distance between the data I/O pin groups DP of the integrated circuits. For example, in the configuration of Figure 5 of Yamasaki, the data line lengths of the data I/O pin groups DP of integrated circuits 1A and 1J differ by the distance between these two data I/O pin groups perpendicular to the center line. In contrast, embodiments of the invention recited by amended Claim 1 are able to reduce the difference between the data line lengths to be significantly smaller than the distance between the corresponding data pins (e.g., to within 10% of the total trace length).

Furthermore, in contrast to the disclosure of Yamasaki, embodiments of the claimed invention provide substantially equal data line lengths for corresponding data lines regardless of the position of the data pin on the integrated circuit. For example, as shown in FIGURE 4A of the present application, embodiments of the claimed invention provide substantially equal data line lengths for data lines connected to corresponding data pins close to the end of the integrated circuit (e.g., data lines 406, 416 have lengths which are substantially equal to one another) and for data lines connected to corresponding data pins closer to the center of the integrated circuit (e.g., data lines 404, 414 have lengths which are substantially equal to one another). By having trace lengths on different interconnection levels, embodiments of the claimed invention achieve substantially equal data line lengths for any of the data pins, not just those nearest the center line of the printed circuit board (as disclosed by Yamasaki).

For the reasons discussed above, Applicants submit that amended Claim 1 is patentably distinguished over Yamasaki. Applicants respectfully request the Examiner to withdraw the rejection of amended Claim 1 and to pass amended Claim 1 to allowance.

Claims 2 and 4-6

Each of Claims 2 and 4 depend from amended Claim 1, and each of Claims 5 and 6 depends from Claim 4. Therefore, each of Claims 2 and 4-6 includes all the limitations of amended Claim 1, as well as other limitations of particular utility. For the reasons discussed above, Applicants submit that each of Claims 2 and 4-6 is patentably distinguished over Yamasaki. Applicants respectfully request the Examiner to withdraw the rejection of Claims 2 and 4-6 and to pass these claims to allowance.

Claim 8

Applicants have amended independent Claim 8. For the reasons stated above with respect to amended Claim 1, Applicants submit that amended Claim 8 is patentably distinguished over Yamasaki. Applicants respectfully request the Examiner to withdraw the rejection of amended Claim 8 and to pass amended Claim 8 to allowance.

Claims 9-12

Each of Claims 9 and 10 depend from amended Claim 8, and each of Claims 11 and 12 depends from Claim 10. Therefore, each of Claims 9-12 includes all the limitations of amended Claim 8, as well as other limitations of particular utility. For the reasons discussed above, Applicants submit that each of Claims 9-12 is patentably distinguished over Yamasaki.

Applicants respectfully request the Examiner to withdraw the rejection of Claims 9-12 and to pass these claims to allowance.

Claim 17

Applicants have amended independent Claim 17. For the reasons stated above with respect to amended Claim 1, Applicants submit that amended Claim 17 is patentably distinguished over Yamasaki. Applicants respectfully request the Examiner to withdraw the rejection of amended Claim 17 and to pass amended Claim 17 to allowance.

Claims 18 and 19

Each of Claims 18 and 19 depends from amended Claim 17. Therefore, each of Claims 18 and 19 includes all the limitations of amended Claim 17, as well as other limitations of particular utility. For the reasons discussed above, Applicants submit that each of Claims 18 and 19 is patentably distinguished over Yamasaki. Applicants respectfully request the Examiner to withdraw the rejection of Claims 18 and 19 and to pass these claims to allowance.

Response to Rejection of Claims 7, 13-16, and 20 Under 35 U.S.C. § 103(a)

In the August 19, 2004 Office Action, the Examiner rejects Claims 7, 13-16, and 20 under 35 U.S.C. § 103(a) as being unpatentable over Yamasaki in view of U.S. Patent No. 6,502,161 issued to Perego et al. ("Perego"). The Examiner states that Yamasaki discloses all the limitations of Claims 7, 13-16, and 20, except for "a first common register for the ICs on the first lateral half, a second common register for the ICs on the second half." The Examiner further states that Perego discloses a buffer for accessing the ICs in a combined fashion, and that it would be obvious to one of ordinary skill in the art to realize all the variations of design as exemplified by the claimed features from the disclosure of Perego.

As discussed above, Applicants submit that amended Claims 1, 8, and 17 each includes limitations that are not taught or suggested by Yamasaki. Applicants submit that the limitations of these claims which are missing from Yamasaki are not taught or suggested by Perego. Therefore, Applicants submit that amended Claims 1, 8, and 17 are patentably distinguished over the combination of Yamasaki in view of Perego.

Claim 7

Claim 7 depends from Claim 4, which depends from amended Claim 1. Therefore, Claim 7 includes all the limitations of amended Claim 1, as well as other limitations of particular utility. Applicants submit that Claim 7 is patentably distinguished over Yamasaki in view of

Perego. Applicants respectfully request that the Examiner withdraw the rejection of Claim 7 and to pass Claim 7 to allowance.

Claims 13-16

Claim 13 depends from Claim 10, which depends from amended Claim 8. Claim 14 depends from amended Claim 8, and each of Claims 15 and 16 depends from Claim 14. Therefore, each of Claims 13-16 includes all the limitations of amended Claim 8, as well as other limitations of particular utility. Applicants submit that each of Claims 13-16 is patentably distinguished over Yamasaki in view of Perego. Applicants respectfully request that the Examiner withdraw the rejection of Claims 13-16 and to pass Claims 13-16 to allowance.

Claim 20

As described herein, Applicants have amended Claim 20 to depend from Claim 19, which depends from amended Claim 17. Therefore, Claim 20 includes all the limitations of amended Claim 17, as well as other limitations of particular utility. Applicants submit that Claim 20 is patentably distinguished over Yamasaki in view of Perego. Applicants respectfully request that the Examiner withdraw the rejection of Claim 20 and to pass Claim 20 to allowance.

Summary

For the foregoing reasons, Applicants submit that Claims 1, 2, and 4-20 are in condition for allowance, and Applicants respectfully request such action.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

Dated: 11/16/04 By: _____

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